CLAIMS

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1. An apparatus comprising:

a first circuit configured to wake-up a second circuit in response to an input signal, wherein said input signal comprises a programmable delay value.

2. The apparatus according to claim 1, wherein said input signal comprises a user programmable signal.

3. The apparatus according to claim 1, wherein said input signal comprises a multi-bit signal.

4. The apparatus according to claim 1, wherein said delay value comprises a programmable delay value.

5. The apparatus according to claim 1, wherein said delay value comprises a wake-up timing value.

6. The apparatus according to claim 1, wherein said first circuit comprises:

a delay circuit configured to present a first delay signal; and

a select circuit configured to present a second delay signal in response to said first delay signal, wherein said second delay signal is configured to wake-up said second circuit.

7. The apparatus according to claim 6, wherein said input signal is configured to control a programmable delay of said second delay signal.

8. The apparatus according to claim 7, wherein said programmable delay comprises a multiple of said first delay signal.

9. The apparatus according to claim 6, wherein said select circuit is further configured in response to said input signal.

10. The apparatus according to claim 6, wherein said select circuit comprises:

a divider circuit configured to present one or more divided signals in response to said first delay signal; and

a multiplexer configured to present said second delay signal in response to said one or more divided signals and said input signal.

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11. The apparatus according to claim 6, wherein said select circuit comprises a counter configured to generate said second delay signal in response to said input signal.

12. The apparatus according to claim 6, wherein said delay circuit is further configured to present said delay signal in response to an enable signal.

13. The apparatus according to claim 1, wherein said input signal is generated in response to a device selected from the group consisting of input pins, data pins, microprocessor code, and firmware.

14. An apparatus comprising:

a first circuit configured to operate in a first mode or a second mode; and

a second circuit configured to control switching of said first circuit from said first mode to said second mode after a programmable period of time.

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15. A method for wake-up timing comprising the steps of:

(A) receiving an input signal; and

(B) waking-up a circuit in response to said input signal, wherein said input signal comprises a programmable delay value.

16. The method according to claim 15, wherein said input signal comprises a user programmable signal and said delay value comprises a programmable delay value.

17. A computer readable medium containing instructions to execute the steps of claim 15.

18. The method according to claim 15, wherein step (B) further comprises the sub-steps of:

(B-1) presenting a first delay signal; and

(B-2) presenting a second delay signal in response to said first delay signal, wherein said second delay signal is configured to wake-up said circuit.

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19. The method according to claim 18, wherein step (B) further comprises the sub-step of:

(B-3) controlling a programmable delay of said second delay signal.

20. The method according to claim 15, further comprising the step of:

(C) generating said input signal in response to input pins, data pins, microprocessor code, and/or firmware.

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